



IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: M. Riedel *et al.*
Serial No.: 10/728,570
Filed: December 5, 2003
Customer No.: 33123
For: SYNTHESIS OF CYCLIC
COMBINATIONAL CIRCUITS
Art Unit: 2819
Examiner: Unknown

CERTIFICATE OF MAILING PURSUANT TO 37 CFR 1.8

I hereby certify that this correspondence and the attached papers are being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated below in an envelope addressed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

8-26-04
Date

Melinda Melander
Signature

INFORMATION DISCLOSURE STATEMENT
IN ACCORDANCE WITH 37 C.F.R. §§ 1.97-1.98

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Because this Information Disclosure Statement is filed prior to receipt of a First Office Action on the merits of the above-captioned application, a fee for filing this statement should not be due. If, however, it is determined that a fee is due, then any fees that may be due in connection with filing this paper may be charged to Deposit Account No. 50-1213.

In accordance with the duty of disclosure imposed by 37 C.F.R. § 1.56 to inform the Patent Office of all material references known by Applicant or Applicants' representative, this Information Disclosure Statement prepared in accordance with 37 C.F.R. §§ 1.97-1.98 is hereby submitted. The Form PTO/SB/08B (PTO-1449) (1 page) is provided herewith for filing in connection with the above cited application. A copy of the non-patent documents is provided, per 37 C.F.R. § 1.98(a)(2).

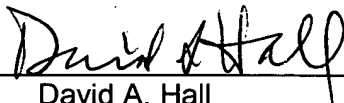
The document(s) cited on the Form PTO-1449 are in the English language. Hence, in accordance with the requirements of 37 C.F.R. § 1.98, as amended effective March 16, 1992, no further explanation of the listed items is necessary.

Although these documents and information are made known to the Patent and Trademark Office in compliance with Applicants' duty of disclosure, such

disclosure is not to be construed as an admission by Applicants or Applicants' representative that any of the references, singly or in any combination thereof, is effective as prior art against the subject application. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(b) exists.

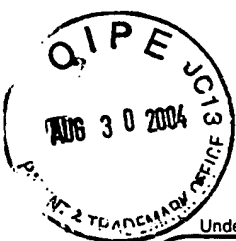
Applicants respectfully request that the Examiner review the foregoing references and request that they be made of record in the file history of the above-captioned application.

Respectfully submitted,
HELLER, EHRMAN, WHITE & McAULIFFE LLP

By: 

David A. Hall
Registration No. 32,233

Address all correspondence to:
David A. Hall
HELLER EHRMAN WHITE & McAULIFFE LLP
4350 La Jolla Village Dr., 7th Floor
San Diego, CA 92122-1246
Telephone: (858) 450-8400
Facsimile: (858) 450-8499
EMAIL: dhall@hewm.com



PTO/SB/08B (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	10/728,570		
		Filing Date	12/05/2003		
		First Named Inventor	M. Riedel		
		Art Unit	2819		
		Examiner Name	Not yet assigned		
Sheet	1	of	1	Attorney Docket Number	18021-6226

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A	R. Brayton et al., Logic Minimization Algorithms for VLSI Synthesis, Chapter 7, "Comparisons and Conclusions", pp. 160-173, 1984.	
	B	J. Brzozowski et al., Asynchronous Circuits, Chapter 6, "Up-Bounded-Delay Race Models", pp. 83-111, 1994.	
	C	J. Brzozowski et al., Asynchronous Circuits, Chapter 15, "Design of Asynchronous Circuits", pp. 314-367, 1994.	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO:**
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.